

EXPERIMENT REPORT

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| **Experiment Name** | Logic Gates and Multivibrators |
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|  | 31.10.2014 |  |

**EXPERIMENT 6**

**Logic Gates and Multivibrators**

**Purpose of the experiment**

In this experiment, the basic logic Gates will be investigated and the principle of operations for monostable and bistable circuits will be observed.

**The Benefits of Experiment**

* The truth tables of logic gates and ability to predict outputs without looking at the table
* The meaning of “0” and “1” in logic circuits
* Flip-flop circuits their uses
* Ability to analyze the monostable circuit like that way explained in the documentation
* Understanding how and why a node voltage can exceed the supply voltage
* The purpose of ESD diodes in I/Os of integrated circuits and the effects of those diodes in the experiments
* Constructing the circuit on a cadet board

**Experiment 6.1:**

At the beginning the experiment, the behavior of the NAND gate, which is composed of 4 transistors, is analyzed with respect to its two inputs and one output by watching the position of the red LEDs (ON or OFF). NAND gate works as the invers of AND operation. Therefore, the output is only ‘0’ when all the inputs are ‘1’. Otherwise, output is ‘1’.

A

B

Y

NAND Gate

Then, all the four combinations are done with the inputs (00, 01, 10 and 11) and the truth table at the left side is generated.

|  |  |  |
| --- | --- | --- |
| A | **B** | **Y** |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Experiment 6.3:**

At the second step, NOT gate and AND gate are investigated for all possible input configurations. NOT gate is implemented by connecting both inputs of NAND gate at the same point. The output of NOT gate is read the inverse of the input. Therefore, when input is ‘1’, output has to be ’0’ or vice versa. The truth table is shown below.

A

B

Y

|  |  |
| --- | --- |
| A | Y= A’ |
| 0 | 1 |
| 1 | 0 |

AND gate is implemented one NAND gate and its inverse (same input NAND gate at previous section).

|  |  |  |
| --- | --- | --- |
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

A

B

Y

AND gate

**Experiment 6.4:**

Q’

Q

**SR latch**

S

R

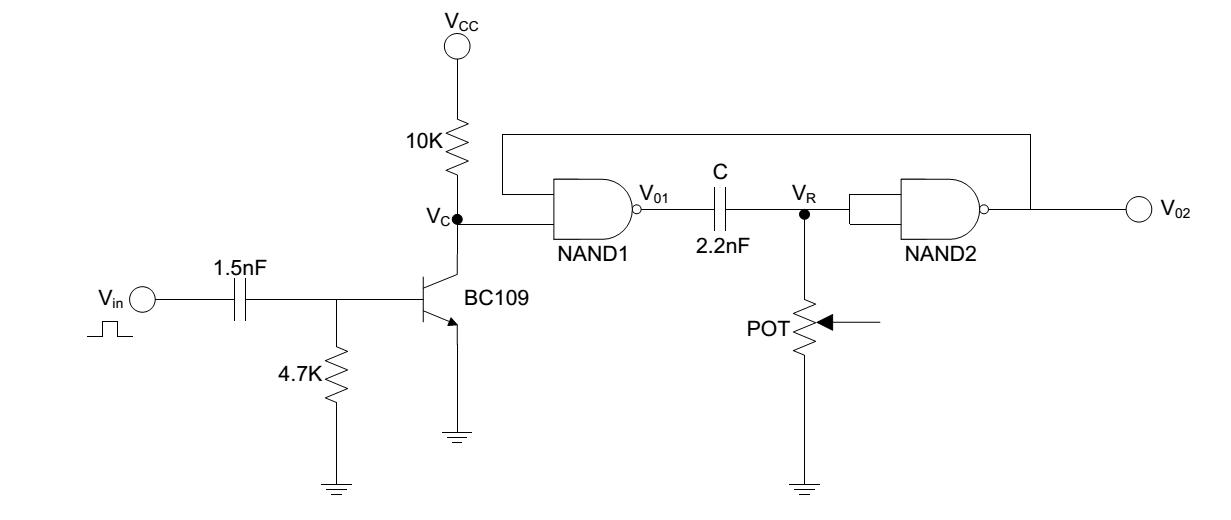
In this section SR latch circuit is constructed with NAND gates.

SR latch is a flip-flop circuit that both stores the information its inside given before and writes the information for the desired input at one time. There are two inputs to (S) set and (R) reset and two outputs Q and Q’ (inverse of Q).

|  |  |  |  |
| --- | --- | --- | --- |
| S | R | Q | Q' |
| 0 | 0 | Forbidden State | |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | **Memory(previous value)** | |

**Experiment 6.4:**

At the last part of the experiment, monostable vibrator - the circuit shown below- is built. Then the voltage characteristics of two points which are Vc and VR are plotted on the protocol sheet.



The collector node of the transistor is triggered to ‘0’ in a very closed intervals due to the C1 capacitor (1.5nF at the input side). In that interval, the VR reaches the maximum values and after that it starts to discharge due to the C2 capacitor (2.2nF).

When VR is equal to the logic 1, Vo2 equals to logic 0 due to the inverter. After that, VR starts to decrease due to the effect of C2 capacitor and when it is below than half of the supply of the NAND gate (in the experiment it is 1.8V) Vo2 forced to be logic 0 and it makes Vo1 and also VR logic 0 due to the NAND gate.